Analyzing Sub-threshold Bitcell Topologies and the Effects of Assist Methods on SRAM V_{MIN} (November 2011)

James Boley, *Member, IEEE*

***Abstract*—The need for ultra low power circuits has forced circuit designers to scale voltage supplies into the sub-threshold region where energy per operation is minimized [1]. The problem with this is that the traditional 6T SRAM bitcell, used for data storage, becomes unreliable at voltages below 700 mV due to process variations and decreased device drive strength [3]. In order to achieve reliable operation, new bitcell topologies and assist methods have been proposed. This paper provides a comparison of four different bitcell topologies using read and write V_{MIN} as the metrics for evaluation. In addition, read and write assist methods were tested using the periphery voltage scaling techniques discussed in [3-6]. Measurements taken from a 180 nm test chip show read functionality, without assist methods, down to 500 mV and write functionality down to 600 mV. Using assist methods both read and write V_{MIN} can be reduced by 100 mV from the unassisted test case.**

***Index Terms*—Subthreshold design, assist methods, alternative bitcell topologies**

I. INTRODUCTION

As mobile devices become heavily energy constrained, the need for ultra low power circuits has emerged. In order to reduce energy consumption, voltage supplies are scaled down, resulting in quadratic energy savings. The sub-threshold region ($V_{DD}<V_T$) has been shown by [1] to minimize energy per operation. Sub-threshold systems require Static Random Access Memory (SRAM) for storing data at these low voltages. The problem is that while logic has been shown to easily scale into the sub-threshold region, the traditional 6T SRAM bitcell becomes unreliable at voltages below 700 mV due to process variations and decreased device drive strength [3]. SRAM devices are typically minimum sized, which further compounds this problem. As the capacity of SRAM arrays continues to increase, the stability (typically measured in terms of Static Noise Margin (SNM) [2]) of the worst case bitcell degrades. Therefore in order for the minimum operating voltage (V_{MIN}) of SRAMs to enter the sub-threshold regime, more robust bitcell designs and assist methods must be used.

One possible solution to this problem is to design a more robust bitcell topology capable of larger read and write margins. The downside to this strategy is that adding more transistors to the bitcell increases the total area of the array. The second strategy is to use various assist methods [3-6] to make the cell easier to read and write. This method also results in an area overhead and requires multiple voltage sources. In this work we will analyze the different bitcell topologies and assist methods to determine which is the most effective at reducing SRAM V_{MIN}. In section II, we will introduce a variety of sub-threshold bitcell topologies and explain the pros and cons of each. In section III we will explain the need for read and write assist methods, and how each method can be used to improve margins. Section IV will present the results from a test chip and Section V will conclude.

II. INTRODUCTION OF SUB-THRESHOLD BITCELL TOPOLOGIES

In a sub-threshold circuit, the supply voltage (V_{DD}) is set below the threshold voltage (V_T) of the transistors. This reduction in V_{DD} results in a quadratic reduction in dynamic power. In addition, it reduces leakage power which is especially important for SRAMs, which typically contain thousands of bitcells. The main limitations of sub-threshold circuits are their sensitivity to variation and slow speed. In the sub-threshold region, transistor currents vary exponentially with V_T. This makes designing ratioed circuits such as SRAMs nearly impossible. Another problem is that the I_{on}/I_{off} current ratio is reduced which can lead to read access failures. In order to combat these problems, new bitcell topologies have been introduced and are described below.

The 8T bitcell shown in Fig. 1 a adds a two transistor read buffer

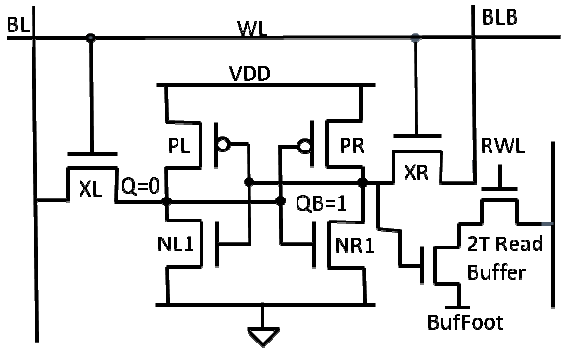


Fig. 1 The 8T bitcell uses a buffer to improve read SNM

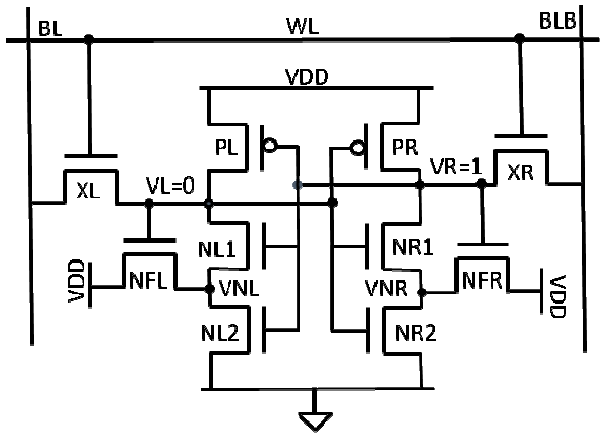


Fig. 2 The 10T ST bitcell schematic

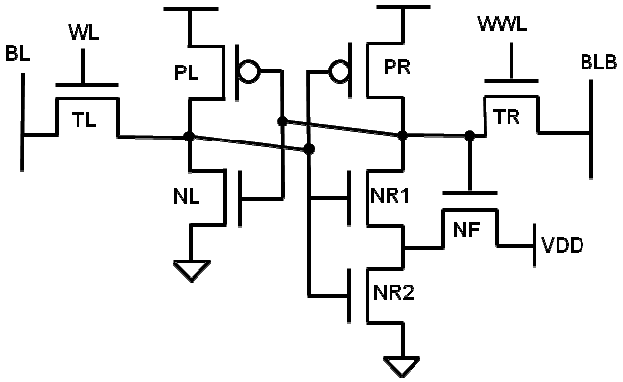


Fig. 3 The 8T asymmetric ST bitcell schematic

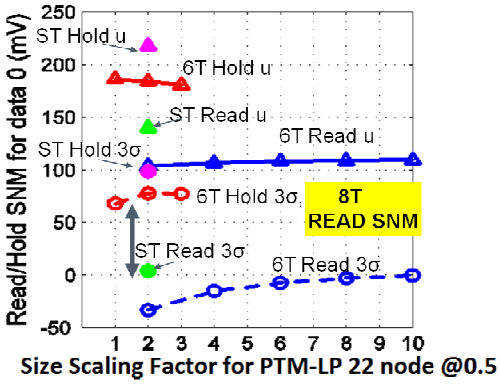


Fig. 4 Comparison of read and hold SNMs

to the conventional 6T bitcell in order to prevent the data from being disturbed during a read. In a normal read operation, the bitlines are precharged and the WL is pulsed high, causing the bitcell to discharge one of the bitlines. The problem with this is that if the node storing a '0' rises above the V_T of the NR1 device, then the cell could unintentionally flip. The 8T cell solves this problem by decoupling the data from the read operation; therefore the read SNM becomes the hold SNM. One weakness of this bitcell is that it still suffers from half-select instability, which occurs during a write when an unselected cell is 'read'. Currently the best method to solve this problem is to read the entire row and then write the data back into the unselected cells.

The 10T bitcell (Fig. 2) uses Schmitt Trigger (ST) inverters to help improve the read static noise margin (RSNM). The NR2/NFR feedback transistors weaken the pull down network when VR is high, increasing the switching threshold of the right inverter. This means that the VL node would have to pull up much higher during a read in order to flip the cell, resulting in higher read stability. The downside to this topology is that the four extra transistors result in a 33% area penalty compared to the 6T bitcell.

The novel design presented in this work is the 8T asymmetric Schmitt Trigger bitcell (Fig. 3). This bitcell uses single-ended reading and asymmetric inverters, similar to the 5T bitcell [7] to improve read margin. The WL is pulsed high during both a read and write, and the WWL is only pulsed high during a write. In simulation this bitcell achieves 86% higher RSNM than the 6T cell and 19% higher RSNM than the 10T ST bitcell.

A comparison between the 6T, 8T, and 10T ST bitcells is provided in Fig 4. The first thing to notice is that the 8T bitcell has the best read SNM, which is the same as the 6T hold SNM. Also, the ST bitcell has the best hold SNM, but its read SNM is not as good as the 8T's. The third take away from this figure is that increasing the size of the 6T bitcell (x-axis) does not result in significant improvements in the read SNM.

III. Introduction of Read and Write Assist Methods

A. *Write Assist Methods*

A write failure occurs when value being stored in the bitcell is unable to be flipped. For example, to write the bitcell in Fig. 1, the bitline (BL) is held high and BLB is held low. In order for the internal state to flip, pass-gate transistor XR must be able to pull node QB below the switching threshold of the left inverter. A ratioed fight is occurring between XR and PR, therefore transistor PR is usually made weak, to make writing easier.

The goal of write assist methods is to further weaken the pull-up transistor or strengthen the pass-gate transistor. There are several ways to accomplish this. The first is to increase the pass-gate to pull-up ratio, however because we are operating in sub-threshold this is not an efficient knob. The second method is to collapse V_{DD}, which weakens the pull-up transistors. The third and fourth methods involve strengthening the pass-gate transistors by either boosting the WL V_{DD} or reducing the BL V_{SS}. These methods strengthen the passgate by increasing its V_{GS}. The downside to boosting the WL V_{DD} is that it reduces half selected cell stability. The weakness of reducing the BL V_{SS} is that it results in increased BL leaking.

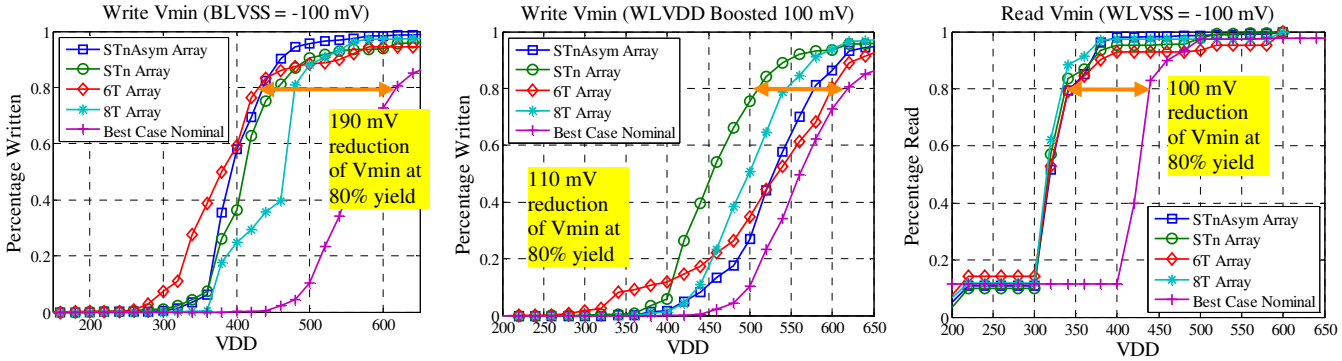
B. *Read Assist Methods*

Read failures can occurs in two ways. The first is that the bitcell is flipped during a read operation (referred to as read stability). This can occur when the XL and NL1 transistors (Fig. 1) are sinking the large amount of charge from the highly capacitive BL, and the Q node rises above the trip point of the right inverter. In order to increase read stability, the pull-down transistor is made stronger than the pass-gate. The second type of read failure occurs when the voltage difference between the BL and BLB is not large enough for the sense amp to determine the correct value (referred to as read access). This happens in sub-threshold especially due to the BL leakage current in unaccessed cells causing the BL voltage to droop.

There are two goals involved in read assist methods. The first is to improve the stability of the cross-coupled inverters during the read by either raising the bitcell V_{DD} or reducing its V_{SS}. While raising bitcell V_{DD} has been shown by [3] to result in larger gains in RSNM, the advantage of reducing the bitcell VSS is that it significantly reduces read delay due to the body effect strengthening both the pull-down and pass-gate transistors. The second goal is improve read access by increasing the read current (I_{on}) and reducing the BL leakage in unaccessed cells (I_{off}). The read current can be increased by boosting the WL V_{DD}. The downside here is that by strengthening the passgate, you reduce the stability of the cross-coupled inverters. In order to reduce bitline leakage current the WL V_{SS} is reduced to a negative voltage.

IV. Results

Because the test chip was fabricated during the first run of a new technology (MITLL 180nm FDSOI), the yield was not ideal. We found full columns to be non-functional as well as a relatively large number of random bit failures. However, even with the non-ideal yield we were able to obtain some interesting results. The first interesting result was that the SRAM proved to be write limited, meaning that the write V_{MIN} exceeded the read V_{MIN}. The best case write V_{MIN} at 80% yield was 620 mV, and the best case read V_{MIN} was 440 mV at 80% yield. The 8T bitcell offered the lowest read V_{MIN} which is surprisingly only 10% lower than the other three bitcells. This is interesting because in simulation, the RSNM of the



a) b) c)

Fig. 5(a) effect of BL V_{SS} reduction on write V_{MIN} (b) effect of WL V_{DD} boosting on write V_{MIN} (c) effect of WL V_{SS} reduction on read V_{MIN}

asymmetric ST and 10T ST bitcells was much higher than the 6T bitcell. What we would was that there seems to be a discrepancy between the spice models and silicon data. This is most likely due to the technology being relatively immature at this point.

Table 1 Comparison of Write Assist Methods

Bitcell	BLVSS	WLVDD
6T	30%	3%
8T	23%	12%
10T ST	27%	18%
Asym. ST	30%	7%

The results from the different write assist methods are shown above in Table 1 and Fig. 5(a-b). Based on these figures, we can conclude that BL V_{SS} reduction is the most effect method for reducing write V_{MIN}. This method outperforms the WL V_{DD} boost method across each of the bitcells. It is interesting to note that the 6T bitcell and Asymmetric ST bitcell achieve the lowest write V_{MIN} at 430 mV, a reduction of 190 mV compared to the best case without assist methods.

As seen in Fig. 5c, the WL V_{SS} reduction resulted in a 100 mV reduction in read V_{MIN} for each of the bitcells. The interesting trend with this plot is that each of the bitcells had almost identical read V_{MIN} values. This would suggest using a combination of the 6T bitcell and WL VSS reduction is the most area efficient strategy for reducing read V_{MIN}. Based on the results from Fig. 6, reducing WL V_{SS} and bitcell V_{SS} consistently improved the read V_{MIN} for each of the bitcells. This suggests that bitline leakage was a major contributor to reduced read margin. It is also interesting to note that increasing the bitcell V_{DD} had the greatest impact on the 10T ST bitcell and WL V_{DD} boosting had the most positive effect on the 8T bitcell.

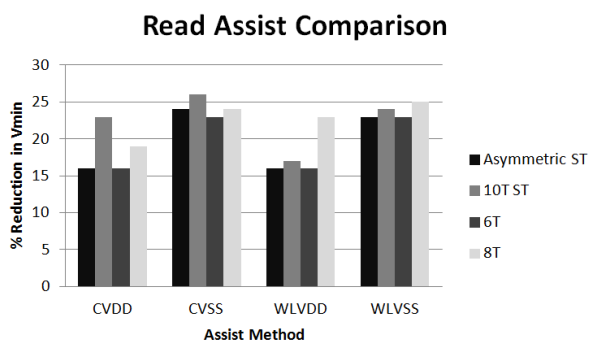


Fig. 6 Comparison of the different read assist methods

V. Conclusion

Although the asymmetrical ST and 10T ST bitcells showed higher RSNM in simulation, silicon results showed read V_{MIN} comparable to the 6T bitcell. Therefore it would be interesting to repeat this analysis in a more mature technology, to determine if the discrepancy was caused by the Spice models or by faults in the immature process. Sub-threshold bitcells proved to be write-limited, with unassisted write V_{MIN} 41% higher than read V_{MIN}. This trend has been shown by [8] to be especially true in newer technologies. In terms of write assist methods, the BL V_{SS} reduction is the most effective, providing a 46% increase at -200 mV. Reducing WL V_{SS} or bitcell V_{SS} provided the largest reduction in read V_{MIN} of 26%. Based on our results, we can conclude that using assist methods as opposed to designing new bitcell topologies is more effective at reducing SRAM V_{MIN}.

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